

研发产品测试 - 功能 #1227

QOS不同优先级业务功能支持

2023-07-19 18:32 - 匿名用户

状态:	已解决	开始日期:	2023-07-19
优先级:	普通	计划完成日期:	
指派给:		% 完成:	0%
类别:		预期时间:	0.00 小时
目标版本:		耗时:	0.00 小时
问题归属:	DU	FPGA板卡类型:	
发现问题版本:	Rel_2.1.14P	CPU类型:	
目标解决问题版本:	Rel_2.1.15P		

描述
对于客户要求的视频流和UDP灌包业务，区分不同的QOS，保证视频流的流畅

历史记录

#1 - 2023-07-28 11:19 - 匿名用户

- 文件 20230728-111806.jpg 已添加

- 状态从 新建 变更为 进行中

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[07-19 18:26:03.088][DEBUG]rgSCHRSrcDlSchedK0K1:K0 Alloc success ,cellId:1 ueId:17018 cellTime(497:5) pdschTime(497:11) pucchTime(497:18) k0Idx:0 k0:0 dlIdx:31 k1Idx:5 k1:7 remDl
[07-19 18:26:03.088][DEBUG]PDCCH AL PDCCH AL selection for UEID[17018]: selected: LVL1, pdcchCqi:15.000000, threSholdForLVL1:9.000000
[07-19 18:26:03.088][DEBUG]rgSCHCmnAllocPucchRsrcForHARQ: pucchTime[497 18] hqBitSize[1] tmpHqPucchRes[0x7fe39140c150] hqPucchRes[(nil)] resSetIndx[0]
[07-19 18:26:03.088][DEBUG][GENSCH][DL]: Scheduling UE 17018 cell 1 proc 7 for totalBo 2663341
[07-19 18:26:03.088][DEBUG]rgSchDedAllocResAndRateMatch: cellId(1) pdschRsrcIdx(0) minRBReq(1) maxRBReq(96) sfn(497) slot(5) isRetx(0)
[07-19 18:26:03.088][DEBUG]KwWkwwDedUeDatReq: ue[17018] rbId[1] lchId[4] Dequeue rlcDlMsgQ[5] sduCnt[1900]
[07-19 18:26:03.088][DEBUG]rgSCHRSrcDlAllocCwTxRb: ueid[17018] effBo[13322] imcs[23] tbsz[13322] bo[2663341] procId[7] startRb[0] numRb[96] rbsAllc[96] bwAssigned[0] rateMatchInp
[07-19 18:26:03.088][DEBUG]rgSCHRSrcDlAllocTxRb: crntTime[497 5] ue:17018 total:2663341
[07-19 18:26:03.088][DEBUG]rgSCHCmnFillHqPpucch: ue[17018] crntTime[497 5] harqId[7] pucchResIdx[0] pucchResId[4] pucchFrmt[0] harqBitSize[1] cDaiAbs[0] pdcchTime[497 11] pdschTi
[07-19 18:26:03.088][DEBUG]DCI_1_1: PRI: bit len: 3 value: 0 bitIdx:38
[07-19 18:26:03.088][DEBUG]rgSCHLv1UtlFillPdschAllocInfoFrmHqP: ue[17018] crntTime[497 5] harqId[7] rv[0] rbStart[0] numRb[96] pdcchTime[497 11] pdschTime[497 11] pucchTime[497
[07-19 18:26:03.088][DEBUG][GENSCH][DL] crntTime[497 5];TB Dstn Idx 0 TB Size 13322 effAlloc 13322 cellId 1
[07-19 18:26:03.088][DEBUG][GENSCH][DL]:UE 17018 TB Dstn LC 5 Bo 2836 totalbo 2851 rlcHdrEstmt 15
[07-19 18:26:03.088][DEBUG][GENSCH][DL] : cellId 1 Ue 17018 lc 5 schdbo 2851 remBo 0
[07-19 18:26:03.088][DEBUG][GENSCH][DL]:UE 17018 TB Dstn LC 4 Bo 2660505 totalbo 2660520 rlcHdrEstmt 15
[07-19 18:26:03.088][DEBUG][GENSCH][DL] : cellId 1 Ue 17018 lc 4 schdbo 10471 remBo 2650049
[07-19 18:26:03.088][DEBUG][GENSCH][DL]:497 5] cellId 1 UE 17018 totalBo 2650049 tbsz req 13322 effAlloc 0
[07-19 18:26:03.088][DEBUG]kwAssembleSdus: 80 after assembly = 2836 LCID:5 RBID:2 UEID:17018 CELLID:1
[07-19 18:26:03.088][DEBUG]kwUtlSndToLi: Ue[17018] boRptIdx[86] boRpt[2836] sduCnt[2]
[07-19 18:26:03.088][DEBUG]kwAssembleSdus: 80 after assembly = 2708768 LCID:4 RBID:1 UEID:17018 CELLID:1
[07-19 18:26:03.088][DEBUG]kwUtlSndToLi: Ue[17018] boRptIdx[87] boRpt[2708768] sduCnt[1893]
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下行调度

MAC优先调度逻辑信道5 RB ID 2(视频流)的数据

RLC优先组包RBID 2的数据包

DU调度是按着不同逻辑信道的优先级高低给分配的调度后TB size, RLC是按着调度器给定的逻辑信道先后顺序进行组包。并且添加到调度列表的过程考虑了GBR的因素,提高了GBR UE的优先级;所以DU的处理已经满足了QoS不同优先级业务的功能支持。

#2 - 2023-07-28 11:21 - 匿名用户

- 状态从 进行中 变更为 转测试

#3 - 2023-10-23 10:40 - 匿名用户

- 状态从 转测试 变更为 已解决

文件

20230728-111806.jpg	668 KB	2023-07-28	匿名用户
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