研发产品测试 - 错误 #2157

【15p_pre2_T4】上行ftp和UDP都出现了MAC调度大包、小包交错出现的情况

2024-09-13 18:51 - 刘 抒放

状态:	进行中	**开始日期:**	2024-09-13
优先级:	普通	**计划完成日期:**	
指派给:	周 立伟	**% 完成:**	0%
类别:		**预期时间:**	0.00 小时
目标版本:		**耗时:**	0.00 小时
问题归属:	DU	**FPGA板卡类型:**	
发现问题版本:	Rel_2.1.15P	**CPU类型:**	
目标解决问题版本:	Rel_2.1.15P		

描述

上行ftp和UDP都出现了MAC调度大包、小包交错出现的情况，直接导致PHY挂死

历史记录

#1 - 2024-10-29 17:18 - 高 峰

- 主题 从 【15p_pre2_T4】上行ftp和UDP都出现了MAC调度大包、小包交错出现的情况，直接导致PHY挂死 变更为 【15p_pre2_T4】上行ftp和UDP都出现了MAC调度大包、小包交错出现的情况

#2 - 2024-10-29 17:19 - 高 峰

初步原因UE上报的BSR不足
1472包长时易出现，计划减少包长再观察一下是否出现

#3 - 2024-12-30 16:47 - 匿名用户

- 状态 从 新建 变更为 挂起

该问题在北京使用DU最新版本16pPre1_T1版本复测包长1472和1400的上行udp灌包，查看最新日志后发现未出现bsr不足和大小包交替的问题；
与测试沟通后该问题暂时挂起，待复现后继续定位。

#4 - 2024-12-31 16:18 - 匿名用户

- 文件 image.jpg 已添加

该问题复现，查看日志后发现在1400包长下也会偶现该问题，如下图所示在9:03分的时候出现上报bsr不足调度RB不够265的现象：

```
Line 725921: [12-30 17:09:03.502][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[931 0] ue[17025] ulBo[15434] rbReq[223]
Line 725938: [12-30 17:09:03.502][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[931:1] puschTime[931:15] tbSz[18447] imcs[23] k2Index[2] startsymb[0] symbnum[13] startrb[4] rbnum[265] modorder[6] dmrsPortNum[1] portsBitMap[1]
Line 725939: [12-30 17:09:03.502][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[931 1] ue[17025] ulBo[107669] rbReq[265]
Line 725956: [12-30 17:09:03.503][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[931:2] puschTime[931:16] tbSz[18447] imcs[23] k2Index[2] startsymb[0] symbnum[13] startrb[4] rbnum[265] modorder[6] dmrsPortNum[1] portsBitMap[1]
Line 725957: [12-30 17:09:03.503][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[931 2] ue[17025] ulBo[89222] rbReq[265]
Line 725970: [12-30 17:09:03.503][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[931:3] puschTime[931:17] tbSz[18447] imcs[23] k2Index[3] startsymb[0] symbnum[13] startrb[4] rbnum[265] modorder[6] dmrsPortNum[1] portsBitMap[1]
Line 725971: [12-30 17:09:03.503][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[931 3] ue[17025] ulBo[70775] rbReq[265]
Line 725984: [12-30 17:09:03.504][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[931:4] puschTime[931:18] tbSz[18447] imcs[23] k2Index[4] startsymb[0] symbnum[13] startrb[4] rbnum[265] modorder[6] dmrsPortNum[1] portsBitMap[1]
Line 725985: [12-30 17:09:03.504][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[931 4] ue[17025] ulBo[52328] rbReq[265]
Line 725998: [12-30 17:09:03.504][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[931:5] puschTime[931:19] tbSz[17422] imcs[23] k2Index[4] startsymb[0] symbnum[13] startrb[18] rbnum[251] modorder[6] dmrsPortNum[1] portsBitMap[1]
Line 725999: [12-30 17:09:03.504][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[931 5] ue[17025] ulBo[33881] rbReq[253]
Line 726013: [12-30 17:09:03.506][DBG_07]DEBUG: UE[17025] Decoded Short BSR, Bsr[28]
Line 726025: [12-30 17:09:03.506][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[931:9] puschTime[932:3] tbSz[16397] imcs[23] k2Index[0] startsymb[0] symbnum[13] startrb[4] rbnum[237] modorder[6] dmrsPortNum[1] portsBitMap[1] u
Line 726026: [12-30 17:09:03.506][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[931 9] ue[17025] ulBo[16459] rbReq[237]
Line 726042: [12-30 17:09:03.507][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[931:10] puschTime[932:4] tbSz[18447] imcs[23] k2Index[1] startsymb[0] symbnum[13] startrb[4] rbnum[265] modorder[6] dmrsPortNum[1] portsBitMap[1]
Line 726043: [12-30 17:09:03.507][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[931 10] ue[17025] ulBo[77254] rbReq[265]
Line 726059: [12-30 17:09:03.507][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[931:11] puschTime[932:5] tbSz[18447] imcs[23] k2Index[2] startsymb[0] symbnum[13] startrb[4] rbnum[265] modorder[6] dmrsPortNum[1] portsBitMap[1]
Line 726060: [12-30 17:09:03.507][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[931 11] ue[17025] ulBo[58837] rbReq[265]
Line 726076: [12-30 17:09:03.508][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[931:12] puschTime[932:6] tbSz[18447] imcs[23] k2Index[2] startsymb[0] symbnum[13] startrb[4] rbnum[265] modorder[6] dmrsPortNum[1] portsBitMap[1]
Line 726077: [12-30 17:09:03.508][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[931 12] ue[17025] ulBo[40390] rbReq[265]
Line 726090: [12-30 17:09:03.508][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[931:13] puschTime[932:7] tbSz[18447] imcs[23] k2Index[3] startsymb[0] symbnum[13] startrb[4] rbnum[265] modorder[6] dmrsPortNum[1] portsBitMap[1]
Line 726091: [12-30 17:09:03.508][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[931 13] ue[17025] ulBo[21943] rbReq[265]
Line 726106: [12-30 17:09:03.509][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[931:14] puschTime[932:8] tbSz[3521] imcs[23] k2Index[4] startsymb[0] symbnum[13] startrb[4] rbnum[51] modorder[6] dmrsPortNum[1] portsBitMap[1] ul
Line 726107: [12-30 17:09:03.509][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[931 14] ue[17025] ulBo[3496] rbReq[51]
Line 726126: [12-30 17:09:03.509][DBG_07]DEBUG: UE[17025] Decoded Short BSR, Bsr[27]
Line 726145: [12-30 17:09:03.511][DBG_07]DEBUG: UE[17025] Decoded Short BSR, Bsr[25]
Line 726159: [12-30 17:09:03.511][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[931:19] puschTime[932:13] tbSz[18447] imcs[23] k2Index[0] startsymb[0] symbnum[13] startrb[4] rbnum[265] modorder[6] dmrsPortNum[1] portsBitMap[1]
Line 726160: [12-30 17:09:03.511][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[931 19] ue[17025] ulBo[55474] rbReq[265]
Line 726177: [12-30 17:09:03.512][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[932:0] puschTime[932:14] tbSz[18447] imcs[23] k2Index[1] startsymb[0] symbnum[13] startrb[4] rbnum[265] modorder[6] dmrsPortNum[1] portsBitMap[1]
Line 726178: [12-30 17:09:03.512][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[932 0] ue[17025] ulBo[28581] rbReq[265]
Line 726183: [12-30 17:09:03.512][DBG_07]DEBUG: UE[17025] Decoded Short BSR, Bsr[22]
Line 726196: [12-30 17:09:03.512][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[932:1] puschTime[932:15] tbSz[10247] imcs[23] k2Index[2] startsymb[0] symbnum[13] startrb[4] rbnum[146] modorder[6] dmrsPortNum[1] portsBitMap[1]
Line 726197: [12-30 17:09:03.512][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[932 1] ue[17025] ulBo[10134] rbReq[146]
Line 726202: [12-30 17:09:03.512][DBG_07]DEBUG: UE[17025] Decoded Long BSR, bsl[0] bs2[0] bs3[0] bs4[0] bs5[0] bs6[0] bs7[0] bs8[0]
Line 726216: [12-30 17:09:03.513][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[932:2] puschTime[932:16] tbSz[10755] imcs[23] k2Index[2] startsymb[0] symbnum[13] startrb[4] rbnum[153] modorder[6] dmrsPortNum[1] portsBitMap[1]
Line 726217: [12-30 17:09:03.513][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[932 2] ue[17025] ulBo[10570] rbReq[153]
Line 726243: [12-30 17:09:03.514][DBG_07]rgSCHSlctrSrInd: ueId[17025] isSrRcvd[0] prioLnk.node[(nil)]
Line 726260: [12-30 17:09:03.514][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[932:5] puschTime[932:17] tbSz[277] imcs[23] k2Index[3] startsymb[0] symbnum[13] startrb[4] rbnum[4] modorder[6] dmrsPortNum[1] portsBitMap[1] ulBo
Line 726261: [12-30 17:09:03.514][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[932 5] ue[17025] ulBo[3] rbReq[1]
Line 726267: [12-30 17:09:03.514][DBG_07]DEBUG: UE[17025] Decoded Short BSR, Bsr[25]
Line 726291: [12-30 17:09:03.515][DBG_07]DEBUG: UE[17025] Decoded Short BSR, Bsr[24]
Line 726295: [12-30 17:09:03.516][DBG_07]DEBUG: UE[17025] Decoded Short BSR, Bsr[24]
Line 726308: [12-30 17:09:03.516][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[932:9] puschTime[933:3] tbSz[18447] imcs[23] k2Index[0] startsymb[0] symbnum[13] startrb[4] rbnum[265] modorder[6] dmrsPortNum[1] portsBitMap[1] u
Line 726309: [12-30 17:09:03.516][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[932 9] ue[17025] ulBo[20516] rbReq[265]
Line 726327: [12-30 17:09:03.517][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[932:10] puschTime[933:4] tbSz[18447] imcs[23] k2Index[1] startsymb[0] symbnum[13] startrb[4] rbnum[265] modorder[6] dmrsPortNum[1] portsBitMap[1]
Line 726328: [12-30 17:09:03.517][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[932 10] ue[17025] ulBo[20516] rbReq[265]
Line 726333: [12-30 17:09:03.517][DBG_07]DEBUG: UE[17025] Decoded Short BSR, Bsr[25]
Line 726348: [12-30 17:09:03.517][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[932:11] puschTime[933:5] tbSz[2112] imcs[23] k2Index[2] startsymb[0] symbnum[13] startrb[4] rbnum[30] modorder[6] dmrsPortNum[1] portsBitMap[1] ul
Line 726349: [12-30 17:09:03.517][DBG_07]rgSCHRsrcUlAllocTxRb: crntTime[932 11] ue[17025] ulBo[2069] rbReq[30]
Line 726362: [12-30 17:09:03.518][DBG_07]rgSCHRsrcUlAllocl CwTxRb: ue[17025] crntTime[932:12] puschTime[933:6] tbSz[18447] imcs[23] k2Index[2] startsymb[0] symbnum[13] startrb[4] rbnum[265] modorder[6] dmrsPortNum[1] portsBitMap[1]
```

查看其它时间点的日志发现，当上报的bsr连续切都为31时上行调度的RB为265，未出现大小RB交替的情况

#5 - 2024-12-31 16:18 - 匿名用户

- 状态 从 挂起 变更为 进行中

#6 - 2025-03-25 15:53 - 周 立伟

- 指派给 从 匿名用户 变更为 周 立伟

文件

image.jpg	1.27 MB	2024-12-31	匿名用户