

2.0基站产品化测试 - 错误 #2660

【2.1.16P_pre1T1】coreset1配成2个symbol，上行误码率达到70%

2025-01-07 12:18 - 郝雷

状态:	已解决	开始日期:	2025-01-07
优先级:	普通	计划完成日期:	
指派给:	郝雷	% 完成:	0%
类别:		预期时间:	0.00 小时
目标版本:		耗时:	0.00 小时
问题归属:	DU	FPGA板卡类型:	
发现问题版本:	Rel_2.1.16P	CPU类型:	
目标解决问题版本:	Rel_2.1.16P		

描述	
基站配置大上行，coreset1配置成2个symbol E500模拟1个UE，接入后灌上下行包，PHY窗口显示的误码率达到70%，上行MCS降为0。 在L1 log里看到在slot3-7，PUSCH功率检测不到， [01-07 12:00:56.631][INFO] Estimated SNR after CE: SlotAdvIdx10635 CRNTI17017-Ant0: --powerbits[5.320] RSRP[-98.278] fEstSnr[-7.024]dB RBStart + RBSIZE463 [01-07 12:00:56.631][INFO] Estimated SNR after CE: SlotAdvIdx10636 CRNTI17017-Ant0: --powerbits[5.308] RSRP[-98.351] fEstSnr[-6.351]dB RBStart + RBSIZE461 [01-07 12:00:56.632][INFO] Estimated SNR after CE: SlotAdvIdx10637 CRNTI17017-Ant0: --powerbits[5.342] RSRP[-98.148] fEstSnr[-6.897]dB RBStart + RBSIZE463 [01-07 12:00:56.632][INFO] Estimated SNR after CE: SlotAdvIdx10638 CRNTI17017-Ant0: --powerbits[8.853] RSRP[-77.011] fEstSnr[18.210]dB RBStart + RBSIZE463 [01-07 12:00:56.633][INFO] Estimated SNR after CE: SlotAdvIdx10639 CRNTI17017-Ant0: --powerbits[8.816] RSRP[-77.230] fEstSnr[18.252]dB RBStart + RBSIZE461 [01-07 12:00:56.634][INFO] Estimated SNR after CE: SlotAdvIdx10643 CRNTI17017-Ant0: --powerbits[5.309] RSRP[-98.345] fEstSnr[-6.547]dB RBStart + RBSIZE463 [01-07 12:00:56.635][INFO] Estimated SNR after CE: SlotAdvIdx10644 CRNTI17017-Ant0: --powerbits[5.314] RSRP[-98.317] fEstSnr[-6.941]dB RBStart + RBSIZE463 [01-07 12:00:56.636][INFO] Estimated SNR after CE: SlotAdvIdx10645 CRNTI17017-Ant0: --powerbits[5.321] RSRP[-98.273] fEstSnr[-7.009]dB RBStart + RBSIZE463 [01-07 12:00:56.636][INFO] Estimated SNR after CE: SlotAdvIdx10646 CRNTI17017-Ant0: --powerbits[5.333] RSRP[-98.203] fEstSnr[-6.487]dB RBStart + RBSIZE463 [01-07 12:00:56.637][INFO] Estimated SNR after CE: SlotAdvIdx10647 CRNTI17017-Ant0: --powerbits[5.323] RSRP[-98.262] fEstSnr[-6.589]dB RBStart + RBSIZE463 [01-07 12:00:56.637][INFO] Estimated SNR after CE: SlotAdvIdx10648 CRNTI17017-Ant0: --powerbits[8.648] RSRP[-78.244] fEstSnr[17.843]dB RBStart + RBSIZE463 [01-07 12:00:56.638][INFO] Estimated SNR after CE: SlotAdvIdx10649 CRNTI17017-Ant0: --powerbits[8.501] RSRP[-79.128] fEstSnr[15.986]dB RBStart + RBSIZE463 [01-07 12:00:56.640][INFO] Estimated SNR after CE: SlotAdvIdx10653 CRNTI17017-Ant0: --powerbits[5.306] RSRP[-98.364] fEstSnr[-6.356]dB RBStart + RBSIZE463 [01-07 12:00:56.640][INFO] Estimated SNR after CE: SlotAdvIdx10654 CRNTI17017-Ant0: --powerbits[5.302] RSRP[-98.387] fEstSnr[-6.670]dB RBStart + RBSIZE463 [01-07 12:00:56.641][INFO] Estimated SNR after CE: SlotAdvIdx10655 CRNTI17017-Ant0: --powerbits[5.327] RSRP[-98.237] fEstSnr[-6.551]dB RBStart + RBSIZE463 [01-07 12:00:56.641][INFO] Estimated SNR after CE: SlotAdvIdx10656 CRNTI17017-Ant0: --powerbits[5.299] RSRP[-98.406] fEstSnr[-6.578]dB RBStart + RBSIZE461 [01-07 12:00:56.642][INFO] Estimated SNR after CE: SlotAdvIdx10657 CRNTI17017-Ant0: --powerbits[5.300] RSRP[-98.401] fEstSnr[-6.820]dB RBStart + RBSIZE463 [01-07 12:00:56.642][INFO] Estimated SNR after CE: SlotAdvIdx10658 CRNTI17017-Ant0: --powerbits[8.725] RSRP[-77.776] fEstSnr[18.059]dB RBStart + RBSIZE463 [01-07 12:00:56.643][INFO] Estimated SNR after CE: SlotAdvIdx10659 CRNTI17017-Ant0: --powerbits[8.743] RSRP[-77.670] fEstSnr[17.653]dB RBStart + RBSIZE461 [01-07 12:00:56.645][INFO] Estimated SNR after CE: SlotAdvIdx10663 CRNTI17017-Ant0: --powerbits[5.303] RSRP[-98.380] fEstSnr[-6.631]dB RBStart + RBSIZE463 [01-07 12:00:56.645][INFO] Estimated SNR after CE: SlotAdvIdx10664 CRNTI17017-Ant0: --powerbits[5.291] RSRP[-98.451] fEstSnr[-6.729]dB RBStart + RBSIZE463 [01-07 12:00:56.646][INFO] Estimated SNR after CE: SlotAdvIdx10665 CRNTI17017-Ant0: --powerbits[5.295] RSRP[-98.427] fEstSnr[-6.399]dB RBStart + RBSIZE463 [01-07 12:00:56.646][INFO] Estimated SNR after CE: SlotAdvIdx10666 CRNTI17017-Ant0: --powerbits[5.304] RSRP[-98.377] fEstSnr[-6.871]dB RBStart + RBSIZE463 [01-07 12:00:56.647][INFO] Estimated SNR after CE: SlotAdvIdx10667 CRNTI17017-Ant0: --powerbits[5.319] RSRP[-98.285] fEstSnr[-6.690]dB RBStart + RBSIZE463 [01-07 12:00:56.647][INFO] Estimated SNR after CE: SlotAdvIdx10668 CRNTI17017-Ant0: --powerbits[8.649] RSRP[-78.237] fEstSnr[18.091]dB RBStart + RBSIZE463	

历史记录

#1- 2025-01-07 14:47 - 匿名用户

- 主题从【2.1.16P_preIT1】coreset1配成2个symbol, 上行速率达到70% 变更为【2.1.16P_preIT1】coreset1配成2个symbol, 上行误码率达到70%

#2- 2025-01-14 15:46 - 匿名用户

- 文件MZTD2NiGOx.jpg 已添加

CORESET1配置2symbol测试：

01-09 15:11:57.409 [FTL_07]rgSCHLWllTomCrcInd:	znti[17063] harqId[7] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[0] usAckNack[1] txCnt[1] rv[0] pusch[809 15] pdccch[809 15] nCCE[49]
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01-09 15:11:57.410 [FTL_07]rgSCHLWllTomCrcInd:	znti[17063] harqId[5] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[1] usAckNack[0] txCnt[1] rv[0] pusch[809 17] pdccch[809 11] nCCE[5]
01-09 15:11:57.411 [FTL_07]rgSCHLWllTomCrcInd:	znti[17063] harqId[2] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[0] usAckNack[1] txCnt[1] rv[0] pusch[809 18] pdccch[809 11] nCCE[5]
01-09 15:11:57.411 [FTL_07]rgSCHLWllTomCrcInd:	znti[17063] harqId[0] numLyrs[1] iMcs[0] zbStart[18] zbNum[251] tbSize[960]	croFail[0] usAckNack[1] txCnt[1] rv[0] pusch[809 19] pdccch[809 12] nCCE[14]
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01-09 15:11:57.419 [FTL_26]rgSCHLWllTomCrcInd:	znti[17063] harqId[8] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[0] usAckNack[0] txCnt[1] rv[0] pusch[810 6] pdccch[810 1] nCCE[27]
01-09 15:11:57.419 [FTL_26]rgSCHLWllTomCrcInd:	znti[17063] harqId[3] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[1] usAckNack[0] txCnt[1] rv[0] pusch[810 7] pdccch[810 1] nCCE[27]
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01-09 15:11:57.428 [FTL_07]rgSCHLWllTomCrcInd:	znti[17063] harqId[15] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[1] usAckNack[0] txCnt[2] rv[2] pusch[811 11] pdccch[811 10] nCCE[23]
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01-09 15:11:57.430 [FTL_26]rgSCHLWllTomCrcInd:	znti[17063] harqId[2] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[0] usAckNack[1] txCnt[1] rv[0] pusch[811 13] pdccch[811 11] nCCE[48]
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01-09 15:11:57.434 [FTL_26]rgSCHLWllTomCrcInd:	znti[17063] harqId[6] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[1] usAckNack[0] txCnt[4] rv[4] pusch[812 5] pdccch[812 0] nCCE[7]
01-09 15:11:57.435 [FTL_26]rgSCHLWllTomCrcInd:	znti[17063] harqId[8] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[1] usAckNack[0] txCnt[3] rv[3] pusch[812 6] pdccch[812 1] nCCE[27]
01-09 15:11:57.435 [FTL_26]rgSCHLWllTomCrcInd:	znti[17063] harqId[3] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[1] usAckNack[0] txCnt[3] rv[3] pusch[812 7] pdccch[812 1] nCCE[27]
01-09 15:11:57.436 [FTL_26]rgSCHLWllTomCrcInd:	znti[17063] harqId[14] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[1] usAckNack[0] txCnt[4] rv[4] pusch[812 8] pdccch[812 1] nCCE[27]
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01-09 15:11:57.439 [FTL_07]rgSCHLWllTomCrcInd:	znti[17063] harqId[15] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[1] usAckNack[0] txCnt[3] rv[3] pusch[812 10] pdccch[812 10] nCCE[23]
01-09 15:11:57.439 [FTL_07]rgSCHLWllTomCrcInd:	znti[17063] harqId[0] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[1] usAckNack[0] txCnt[2] rv[2] pusch[812 11] pdccch[812 10] nCCE[48]
01-09 15:11:57.440 [FTL_26]rgSCHLWllTomCrcInd:	znti[17063] harqId[2] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[0] usAckNack[1] txCnt[1] rv[0] pusch[812 12] pdccch[812 11] nCCE[48]
01-09 15:11:57.440 [FTL_07]rgSCHLWllTomCrcInd:	znti[17063] harqId[1] numLyrs[1] iMcs[0] zbStart[4] zbNum[265] tbSize[1026]	croFail[1] usAckNack[0] txCnt[1] rv[0] pusch[812 13] pdccch[812 11] nCCE[5]
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添加日志后发现同一个slot上分配的CCE存在重叠，从而导致UE解不对PDCCH，进一步导致了高误码的问题；

走读代码发现CCE的分配方式存在问题，从而导致，CCE重复分配的情况；

修改后，E500上高误码问题未出现。

但是2symbol的情况下仍然存在pdccch资源分配失败的情况，待进一步定位

#3- 2025-01-20 09:21 - 匿名用户

- 文件qW4Tmery6z.jpg 已添加

网上查找资料后发现，在多UE场景，这种PDCCH发生冲突属于正常现象，统计128UE的PDCCH分配失败比例，大约为0.1%，认为属于正常现象，对速率以及调度无影响

首先UE要确定搜索空间内PDCCH候选集 (pdccch candidate,即聚合等级AL的pdccch个数)。对于与CORESET p 关联的搜索空间 S (注意: 一个coreset可关联多个ss,而一个ss只对应一个coreset) ,在slot $n_{s,f}^u$ 上, 聚合等级为 L 的PDCCH candidate $m_{s,nci}$, 其起始CCE位置的计算公式如下:

$$L \times \left\{ \left(Y_{P,n_{s,f}^u} + \left\lfloor \frac{m_{s,nci} \times N_{CCE,p}}{L \times M_{s,max}^{(L)}} \right\rfloor + n_{CI} \right) \bmod \left\lfloor N_{CCE,p} / L \right\rfloor \right\} + i$$

聚合等级 L

pdccch candidate 在搜索空间中的起始位置 $m_{s,nci}$

CORESET p 中 CCE 的数目 $N_{CCE,p}$

pdccch candidate的地址 $m_{s,nci}$

聚合等级为 L 的pdccch candidate的数量 $M_{s,max}^{(L)}$

载波指示 n_{CI}

$= 0 \dots L-1$

CSDN @小鸟龟是什么东西啊

- 聚合等级 L : 对于USS, L 可取值1/2/4/8/16; 对于CSS, L 可取值4/8/16; 与LTE相比, NR新增了聚合等级16, 主要目的是通过低的信道编码速率来增加覆盖。
- $Y_{P,n_{s,f}^u}$: 对于CSS, 该值取0, 即对于所有的UE, PDCCH candidate开始的CCE都是相同的。对于USS, PDCCH candidate开始的CCE位置与RNTI有关, 同时随slot变化而变化。这样设计的目的是为了避免两个UE的PDCCH出现持续阻塞的情况。比如, 在某个时刻, 两个UE的PDCCH发生冲突了, 那么在下一个时刻, 通过RNTI随机化后, 这两个UE发送冲突的可能性会大大下降。
- 载波指示 n_{CI} : 在跨载波调度时, 其取值由IE CrossCarrierSchedulingConfig中的高层参数schedulingCellId通知给UE, 以保证调度不同载波的PDCCH candidate时尽可能占用不重叠的CCE。若无跨载波调度 (单载波), 其值取0。另外, 对于CSS, 其值取0。
- $m_{s,nci}$ 表示pdccch candidate的地址, 取值为 $0 \dots M_{s,max}^{(L)} - 1$ 。其中 M 表示服务小区中搜索空间 s 上, 聚合等级为 L 的PDCCH candidate数量。

#4 - 2025-01-21 13:32 - 匿名用户

该问题关联到#2727, 重构pdccch分配部分代码, 计划17P充分验证后和入

#5 - 2025-02-11 15:16 - 匿名用户

解决CCE分配重叠问题, pdccch2symbol高误码问题不再出现

#6 - 2025-02-11 15:16 - 匿名用户

代码落入17P

#7 - 2025-02-11 15:19 - 匿名用户

- 状态从 新建 变更为 转测试
- 指派给从 匿名用户 变更为 郝雷

#8 - 2025-02-11 15:20 - 郝雷

研发给的修复版本上解决, 合入17P。

#9 - 2025-02-11 15:21 - 郝雷

- 状态从 转测试 变更为 已解决

文件

MZTD2NfGOx.jpg	1.46 MB	2025-01-14	匿名用户
qW4Tmery6z.jpg	462 KB	2025-01-20	匿名用户