B5G_UE - 错误 #3821

UU口PUU口PDC DCI1_1的slot号，与基站侧下发的DCI1_1的slot不同，导致L1c计算的PUH上报时机与基站接收时机不一致

2025-07-28 16:52 - 王 金伏

状态:	进行中	**开始日期:**	2025-07-28
优先级:	普通	**计划完成日期:**	
指派给:	王 金伏	**% 完成:**	80%
类别:		**预期时间:**	0.00 小时
目标版本:		**耗时:**	0.00 小时

描述

历史记录

#1 - 2025-07-28 17:02 - 王 金伏

- 文件 20250728-165532.jpg 已添加

- 文件 20250728-165635.jpg 已添加

- 文件 20250728-165723.jpg 已添加

- 文件 20250728-170231.jpg 已添加

- 文件 20250728-170243.jpg 已添加

- 状态 从 新建 变更为 进行中

【问题描述】UU口PUU口PDC DCI1_1的slot号，与基站侧下发的DCI1_1的slot不同，导致L1c计算的PUC上报时机与基站接收时机不一致。

PDC中计算DCI1_1是slot号用到是设备当前的slot号，不是接口带的空口slot。在L1C中计算上报PUC的时机取决于PDC，PUC上报slot = DCI1_1_slot+k1+k0。

```
} « end pdcch_dci_decode_fun »

int32_t phy_gue_dl_pdcch_func(
                                //pdcchCalcParam_t *pdcch_calc_param_ptr,
                                //interface_deofdm_pucch_t *deofdm_param_ptr,
                                PdcchCalcParam_t *pdcch_calc_param_ptr,
                                int32_t *pdcch_malloc_dm0_ptr,
                                int32_t *pdcch_malloc_dm1_ptr,
                                int32_t *pdcch_malloc_dm2_ptr,
                                int32_t *pdcch_malloc_dm3_ptr
                                )
{
    TRACE(SM5_PDCCH_DEBUG_CELL1_ADDR, 0, TRACE_R(SM5_PDCCH_DEBUG_CELL1_ADDR, 0) + 1);

    int32_t pdcchfuncstart,pdcchfuncend;
    pdcchfuncstart = GET_STC_CNT();
    uint16_t slot = get_tx_nr_slot();

    LOG_ERROR_S("0728 111 pdcch_func, slot=%u\n", slot);

    uint16_t sfn = get_rx_nr_sfn();
    int32_t* pdcch_freqdata_ptr = NULLPTR;

    uint32_t mid_value1;
    uint32_t mid_value2;
    uint32_t mid_value3;
    uint8_t air_slot;

    //PdcchDecodeParam_t *decode_param_ptr;
    uint32_t *dma_src_ptr;
    void *mim_ptr;
    pdcch_freqdata_ptr = pdcch_malloc_dm2_ptr;//78624/4 = 19656
    //decode_param_ptr = &pdcch_calc_param_ptr->decodeParam[0];

#if 1
    g_pdcch_freq_data_hdr_dm_ptr->symbol_num=1;
    g_pdcch_freq_data_hdr_dm_ptr->rx_ant_num=1;
    //g_pdcch_freq_data_hdr_dm_ptr->rx_freqdata_ptr=(uint32_t *)g_pdcch_dm3microcfgtab_ptr + g_pdcch_table_param.FREQDATA;
#endif
#if 1
    //dma for freq data
    mid_value1 = g_pdcch_freq_data_hdr_dm_ptr->symbol_num * g_pdcch_freq_data_hdr_dm_ptr->rx_ant_num * (NR_RB_SUBCARRIER_NUM * 4);
    mid_value2 = g_pdcch_freq_data_hdr_dm_ptr->rx_ant_num * (NR_MAX_NUM_PRBS * NR_RB_SUBCARRIER_NUM * 4);
    dma_src_ptr = g_pdcch_freq_data_hdr_dm_ptr->rx_freqdata_ptr;
    air_slot = g_pdcch_freq_data_hdr_dm_ptr->slot;
        // 二维 + 一维DMA频域数据搬移
    // xNumSrc: [源第一维度搬移字节数]       n_prbs * (NR_RB_SUBCARRIER_NUM * 4)
    // yNumSrc: [源第二维度搬移个数]         num_rx_ants
    // yStepSrc:[源第二维度搬移步进字节数]NR_MAX_NUM_PRBS * NR_RB_SUBCARRIER_NUM * 4
    // zStepSrc:[源第三维度搬移步进字节数]mid_value2
    // dataLen: [搬移总字节数]               n_prbs * mid_value1

    ape_csu_dma_3Dto1D_G2L_ch4ch0_simp_transfer((uint32_t)dma_src_ptr,
                                        273 * (NR_RB_SUBCARRIER_NUM * 4),
                                        g_pdcch_freq_data_hdr_dm_ptr->rx_ant_num,
```

终端侧的DCI1_1的slot号，

```
Search "0726" (220 hits in 1 file)
  D:\pucch联调\0724\UU\07263\7-0-str.log (220 hits)
    Line 20: [ERR]0726 pdcchSlotIdx :11  numDci1_1:1  dci1_1->slotIdx:11 numDci1_1:1
    Line 28: [ERR]0726 pdcchSlotIdx :12  numDci1_1:1  dci1_1->slotIdx:12 numDci1_1:1
    Line 31: [ERR]0726 pdcchSlotIdx :11  numDci1_1:2  dci1_1->slotIdx:11 numDci1_1:2
    Line 35: [ERR]0726 pdcchSlotIdx :12  numDci1_1:2  dci1_1->slotIdx:12 numDci1_1:2
    Line 38: [ERR]0726 pdcchSlotIdx :13  numDci1_1:1  dci1_1->slotIdx:13 numDci1_1:1
    Line 45: [ERR]0726 pdcchSlotIdx :11  numDci1_1:3  dci1_1->slotIdx:11 numDci1_1:3
    Line 48: [ERR]0726 pdcchSlotIdx :12  numDci1_1:3  dci1_1->slotIdx:12 numDci1_1:3
    Line 52: [ERR]0726 pdcchSlotIdx :11  numDci1_1:4  dci1_1->slotIdx:11 numDci1_1:4
    Line 56: [ERR]0726 pdcchSlotIdx :12  numDci1_1:4  dci1_1->slotIdx:12 numDci1_1:4
    Line 59: [ERR]0726 pdcchSlotIdx :13  numDci1_1:2  dci1_1->slotIdx:13 numDci1_1:2
    Line 66: [ERR]0726 pdcchSlotIdx :11  numDci1_1:5  dci1_1->slotIdx:11 numDci1_1:5
    Line 69: [ERR]0726 pdcchSlotIdx :12  numDci1_1:5  dci1_1->slotIdx:12 numDci1_1:5
    Line 76: [ERR]0726 pdcchSlotIdx :12  numDci1_1:6  dci1_1->slotIdx:12 numDci1_1:6
    Line 79: [ERR]0726 pdcchSlotIdx :13  numDci1_1:3  dci1_1->slotIdx:13 numDci1_1:3
    Line 86: [ERR]0726 pdcchSlotIdx :11  numDci1_1:6  dci1_1->slotIdx:11 numDci1_1:6
    Line 89: [ERR]0726 pdcchSlotIdx :12  numDci1_1:7  dci1_1->slotIdx:12 numDci1_1:7
    Line 93: [ERR]0726 pdcchSlotIdx :12  numDci1_1:8  dci1_1->slotIdx:12 numDci1_1:8
    Line 96: [ERR]0726 pdcchSlotIdx :11  numDci1_1:7  dci1_1->slotIdx:11 numDci1_1:7
    Line 99: [ERR]0726 pdcchSlotIdx :12  numDci1_1:9  dci1_1->slotIdx:12 numDci1_1:9
    Line 106: [ERR]0726 pdcchSlotIdx :11  numDci1_1:8  dci1_1->slotIdx:11 numDci1_1:8
    Line 114: [ERR]0726 pdcchSlotIdx :12  numDci1_1:10  dci1_1->slotIdx:12 numDci1_1:10
    Line 121: [ERR]0726 pdcchSlotIdx :11  numDci1_1:9  dci1_1->slotIdx:11 numDci1_1:9
    Line 124: [ERR]0726 pdcchSlotIdx :3  numDci1_1:1  dci1_1->slotIdx:3 numDci1_1:1
    Line 127: [ERR]0726 pdcchSlotIdx :12  numDci1_1:11  dci1_1->slotIdx:12 numDci1_1:11
    Line 134: [ERR]0726 pdcchSlotIdx :11  numDci1_1:10  dci1_1->slotIdx:11 numDci1_1:10
    Line 138: [ERR]0726 pdcchSlotIdx :3  numDci1_1:2  dci1_1->slotIdx:3 numDci1_1:2
    Line 141: [ERR]0726 pdcchSlotIdx :12  numDci1_1:12  dci1_1->slotIdx:12 numDci1_1:12
    Line 148: [ERR]0726 pdcchSlotIdx :11  numDci1_1:11  dci1_1->slotIdx:11 numDci1_1:11
    Line 151: [ERR]0726 pdcchSlotIdx :12  numDci1_1:13  dci1_1->slotIdx:12 numDci1_1:13
    Line 158: [ERR]0726 pdcchSlotIdx :11  numDci1_1:12  dci1_1->slotIdx:11 numDci1_1:12
    Line 162: [ERR]0726 pdcchSlotIdx :12  numDci1_1:14  dci1_1->slotIdx:12 numDci1_1:14
    Line 169: [ERR]0726 pdcchSlotIdx :11  numDci1_1:13  dci1_1->slotIdx:11 numDci1_1:13
    Line 172: [ERR]0726 pdcchSlotIdx :12  numDci1_1:15  dci1_1->slotIdx:12 numDci1_1:15
```

基站侧DU的DCI1_1的slot号，

```
7/2025 18:04:20.638][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[5] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[1] rv[0] crntTime[576 3] pdsch[575 10] pucch[575 18]
7/2025 18:04:20.648][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[5] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[2] rv[2] crntTime[577 3] pdsch[576 11] pucch[576 18]
7/2025 18:04:20.658][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[8] imcs[5] rbStart[0] rbNum[8] tbSize[101] Ack/Nack[2] txCntr[1] rv[0] crntTime[578 3] pdsch[577 10] pucch[577 18]
7/2025 18:04:20.658][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[5] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[3] rv[3] crntTime[578 3] pdsch[577 11] pucch[577 18]
7/2025 18:04:20.668][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[8] imcs[5] rbStart[0] rbNum[8] tbSize[101] Ack/Nack[2] txCntr[2] rv[2] crntTime[579 3] pdsch[578 11] pucch[578 18]
7/2025 18:04:20.668][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[5] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[4] rv[1] crntTime[579 3] pdsch[578 12] pucch[578 18]
7/2025 18:04:20.678][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[8] imcs[5] rbStart[0] rbNum[8] tbSize[101] Ack/Nack[2] txCntr[3] rv[3] crntTime[580 3] pdsch[579 10] pucch[579 18]
7/2025 18:04:20.678][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[9] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[1] rv[0] crntTime[580 3] pdsch[579 11] pucch[579 18]
7/2025 18:04:20.688][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[13] imcs[5] rbStart[17] rbNum[6] tbSize[76] Ack/Nack[2] txCntr[1] rv[0] crntTime[581 3] pdsch[580 10] pucch[580 18]
7/2025 18:04:20.688][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[8] imcs[5] rbStart[0] rbNum[8] tbSize[101] Ack/Nack[2] txCntr[4] rv[1] crntTime[581 3] pdsch[580 11] pucch[580 18]
7/2025 18:04:20.688][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[9] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[2] rv[2] crntTime[581 3] pdsch[580 12] pucch[580 18]
7/2025 18:04:20.698][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[13] imcs[5] rbStart[0] rbNum[6] tbSize[76] Ack/Nack[2] txCntr[2] rv[2] crntTime[582 3] pdsch[581 10] pucch[581 18]
7/2025 18:04:20.698][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[9] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[3] rv[3] crntTime[582 3] pdsch[581 11] pucch[581 18]
7/2025 18:04:20.708][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[13] imcs[5] rbStart[0] rbNum[6] tbSize[76] Ack/Nack[2] txCntr[3] rv[3] crntTime[583 3] pdsch[582 11] pucch[582 18]
7/2025 18:04:20.708][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[9] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[4] rv[1] crntTime[583 3] pdsch[582 12] pucch[582 18]
7/2025 18:04:20.718][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[13] imcs[5] rbStart[0] rbNum[6] tbSize[76] Ack/Nack[2] txCntr[4] rv[1] crntTime[584 3] pdsch[583 10] pucch[583 18]
7/2025 18:04:20.718][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[14] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[1] rv[0] crntTime[584 3] pdsch[583 11] pucch[583 18]
7/2025 18:04:20.728][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[14] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[2] rv[2] crntTime[585 3] pdsch[584 11] pucch[584 18]
7/2025 18:04:20.738][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[14] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[3] rv[3] crntTime[586 3] pdsch[585 10] pucch[585 18]
7/2025 18:04:20.748][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[14] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[4] rv[1] crntTime[587 3] pdsch[586 11] pucch[586 18]
7/2025 18:04:20.758][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[15] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[1] rv[0] crntTime[588 3] pdsch[587 10] pucch[587 18]
7/2025 18:04:20.768][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[15] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[2] rv[2] crntTime[589 3] pdsch[588 11] pucch[588 18]
7/2025 18:04:20.773][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[0] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[1] rv[0] crntTime[589 13] pdsch[589 0] pucch[589 8]
7/2025 18:04:20.778][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[15] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[3] rv[3] crntTime[590 3] pdsch[589 10] pucch[589 18]
7/2025 18:04:20.781][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[0] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[0] txCntr[2] rv[2] crntTime[590 10] pdsch[590 2] pucch[590 8]
7/2025 18:04:20.788][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[15] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[4] rv[1] crntTime[591 3] pdsch[590 11] pucch[590 18]
7/2025 18:04:20.793][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[0] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[3] rv[3] crntTime[591 13] pdsch[591 0] pucch[591 8]
7/2025 18:04:20.798][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[1] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[1] rv[0] crntTime[592 3] pdsch[591 10] pucch[591 18]
7/2025 18:04:20.801][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[0] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[0] txCntr[4] rv[1] crntTime[592 10] pdsch[592 2] pucch[592 8]
7/2025 18:04:20.808][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[1] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[2] rv[2] crntTime[593 3] pdsch[592 11] pucch[592 18]
7/2025 18:04:20.818][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[1] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[3] rv[3] crntTime[594 3] pdsch[593 10] pucch[593 18]
7/2025 18:04:20.827][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[1] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[4] rv[1] crntTime[595 3] pdsch[594 11] pucch[594 18]
7/2025 18:04:20.837][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17063] harqId[2] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[2] txCntr[1] rv[0] crntTime[596 3] pdsch[595 10] pucch[595 18]
```

```
result - 228 hits
  Line 2739167: [28/07/2025 11:31:25.837][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17095] harqId[7] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[0] txCntr[4] rv[1] crntTime[409 0] pdsch[408 11] pucch[408 18]
  Line 2739323: [28/07/2025 11:31:25.847][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17095] harqId[9] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[0] txCntr[1] rv[0] crntTime[410 0] pdsch[409 10] pucch[409 18]
  Line 2739466: [28/07/2025 11:31:25.857][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17095] harqId[9] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[0] txCntr[2] rv[2] crntTime[411 0] pdsch[410 11] pucch[410 18]
  Line 2739595: [28/07/2025 11:31:25.867][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17095] harqId[9] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[0] txCntr[3] rv[3] crntTime[412 0] pdsch[411 10] pucch[411 18]
  Line 2739752: [28/07/2025 11:31:25.877][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17095] harqId[9] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[0] txCntr[4] rv[1] crntTime[413 0] pdsch[412 11] pucch[412 18]
  Line 2739912: [28/07/2025 11:31:25.887][DBG_07]rgSCHDhmPrcFdbkForTb: rnti[17095] harqId[11] imcs[5] rbStart[0] rbNum[4] tbSize[48] Ack/Nack[0] txCntr[1] rv[0] crntTime[414 0] pdsch[413 10] pucch[413 18]
```

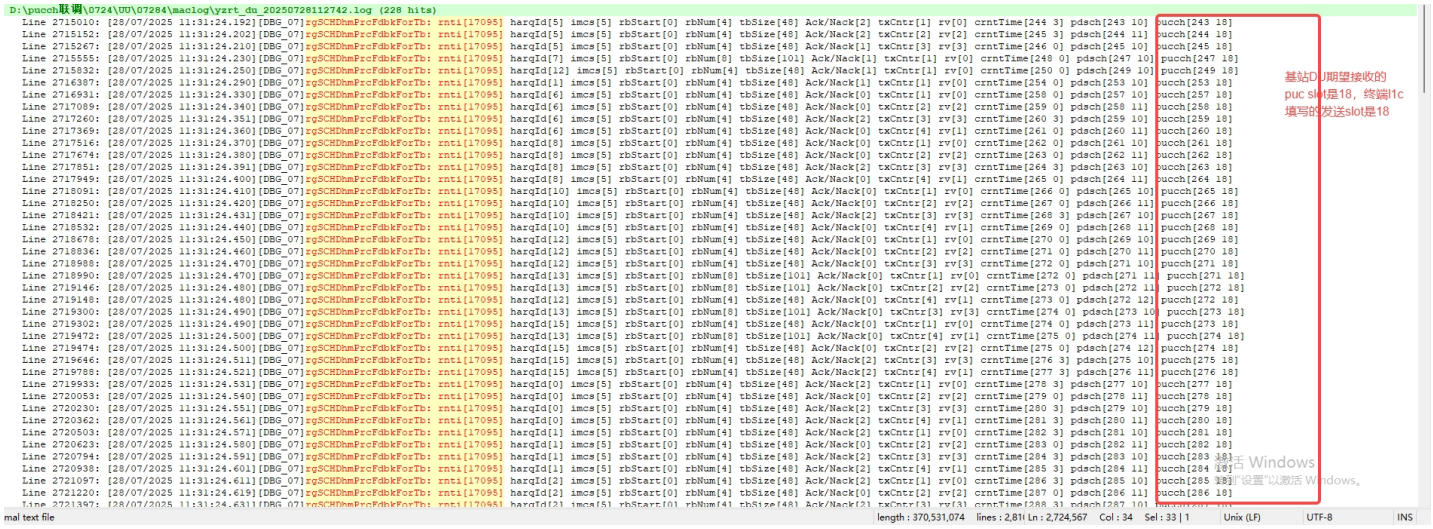
【问题原因】怀疑是PDC应该使用接口中带的airslot作为PDC的DCI1_1的slot，目前PDC中计算DCI1_1是slot号用到是设备当前的slot号，不是接口带的空口slot。

【解决方案】在环境做小版本，将PDC中计算DCI1_1是slot号用接口带的空口slot。在环境验证，终端发送的puc的slot与基站DU侧接收的slot号能对上，但是会出现PDSCH的CRC ERR情况。

```
D:\pucch联调\0724\UU\07284\4-0-str.log (133 hits)
  Line 20: [INFO]L1C fill format0:slotIdx[19] lStart[12] nSym[2] uciPayload[-128] ucipayLoadLen[1] SR[0] csM0[-1660720140]
  Line 33: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[-128] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 45: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[-128] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 57: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[-128] ucipay...  SR[0] csM0[17095]
  Line 66: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[-128] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 75: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[-128] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 84: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[-128] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 96: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[-128] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 105: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[-128] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 117: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[-128] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 126: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[8] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 138: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 147: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 156: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 166: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 179: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucip...
  Line 189: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 202: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 212: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 225: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 235: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 245: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 255: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 268: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 278: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 291: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 301: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 314: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
  Line 324: [INFO]L1C fill format0:slotIdx[18] lStart[13] nSym[1] uciPayload[0] ucipayLoadLen[1] SR[0] csM0[17095]
```

1 ACK

NACK



【问题验证】

#2 - 2025-08-04 13:47 - 王 金伏

- 文件 20250804-104225.jpg 已添加

- 文件 20250804-104608.jpg 已添加

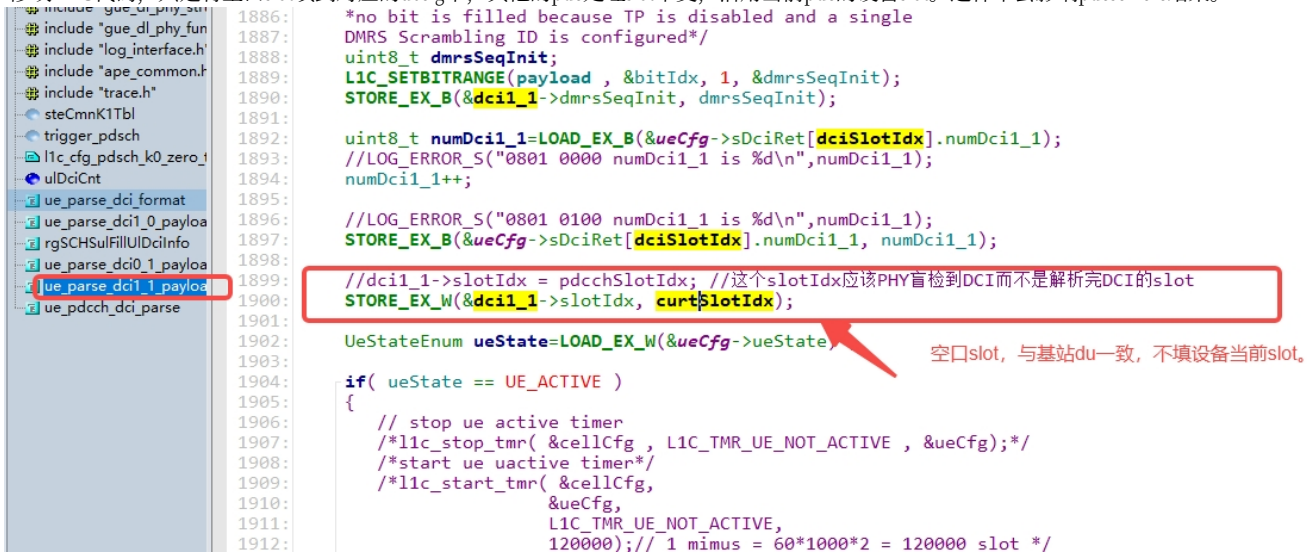
- 文件 20250804-104608.jpg 已添加

- 文件 20250804-104844.jpg 已添加

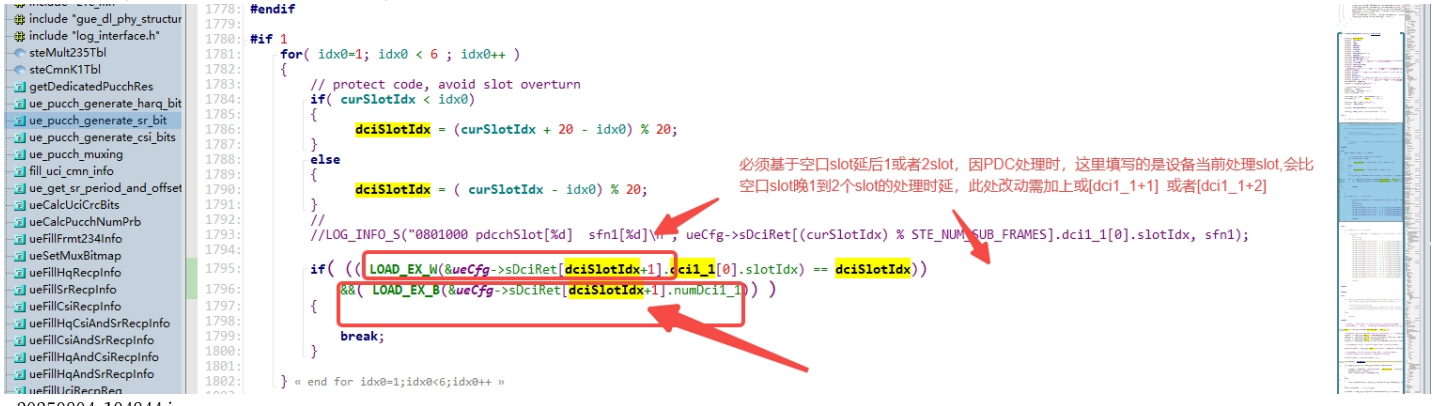
- 文件 20250804-134025.jpg 已添加

- % 完成 从 0 变更为 80

修改PDC代码，只是将空口slot填到对应的uecfg中，其他的pdc处理slot不变，沿用当前pdc的设备slot。这样不会影响pdcsch crc结果。



在L1c中判断空口slot时，必须给当前（slot+1或slot+2）给判断是空口slot。修改后 1
基站DU侧部分NACK是应为PDSCH本身有重传原因，PUC上报的就是NACK；2 DU侧能解析对大部分ACK。（丢失部分dci1_1 slot=0的数据，可能在L1C中清0当时有关，定位中）。



20250804-104844.jpg
20250804-134025.jpg

#3 - 2025-08-04 13:48 - 王 金伏

- 文件 20250804-134025.jpg 已添加

#4 - 2025-08-04 13:51 - 王 金伏

- 文件 已删除 (20250804-134025.jpg)

#5 - 2025-08-04 13:51 - 王 金伏

- 文件 已删除 (20250804-134025.jpg)

文件

20250728-165532.jpg	332 KB	2025-07-28	王 金伏
20250728-165635.jpg	581 KB	2025-07-28	王 金伏
20250728-165723.jpg	1.45 MB	2025-07-28	王 金伏
20250728-170231.jpg	424 KB	2025-07-28	王 金伏
20250728-170243.jpg	1.31 MB	2025-07-28	王 金伏
20250804-104225.jpg	278 KB	2025-08-04	王 金伏
20250804-104608.jpg	282 KB	2025-08-04	王 金伏
20250804-104608.jpg	282 KB	2025-08-04	王 金伏
20250804-104844.jpg	164 KB	2025-08-04	王 金伏