FirstCall - 错误 #3953

msg4后的基站未收到

2025-08-26 17:02 - 赵 强

状态:	进行中	**开始日期:**	2025-08-26
优先级:	普通	**计划完成日期:**	
指派给:	雪峰 赖	**% 完成:**	0%
类别:		**预期时间:**	0.00 小时
目标版本:		**耗时:**	0.00 小时

描述

【问题描述】msg4后的基站PHY未收到
【问题原因】终端在（984,5）上检测到msg4，PUCCH是不会在（984,9）上发数据的，会在（984,9）上发PUCCH。所以基站在（984,9）检测不到。
基站　　终端
msg2(983,10)　　（310,10）接收
msg3(983,19)　　（310,18）发送
msg4(984,5)　　（312,5）　接收
PUCCH（984,,9没有检测到）　　（312,8）此时没有发送PUCCH
基站在这个时刻也不检测PUCCH了　　（313,8）发送PUCCH

对比能解对PUCCH的log看，msg4在（486,1）上终端解对了。然后在（486,9）上基站检到了PUCCH

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[08-26 12:19:21.350][INFO ][TTI_START]: SlotIdx[9719] CellTiming[0]
[08-26 12:19:21.350][INFO ]====================PDSCH tx@(TxFrm[486], SlotNum[1])======================
[08-26 12:19:21.350][INFO ]  nRNTI[17021]  nUEId[0]   BWPSize[98]  nBWPStart[0]  nSubcSpacing[1]  nCpType[0]  nNrOfCodeWords[1]  nMcsTable[0]
[08-26 12:19:21.350][INFO ]  MCS0[8] MCS1[0] TransmissionScheme[0]  NrOfLayers[1]  PortIndex(0-7)[0, 0, 0, 0,  0, 0, 0, 0]
[08-26 12:19:21.350][INFO ]  nNid[41]  nSCID[0]  nNIDnSCID[41]  NrOfAntennaPorts[1]  VRBtoPRB[0]  RBBundleSize[2]  PMI[0]  StartSymbolIndex[1]
[08-26 12:19:21.350][INFO ]=============PUSCH Receive@(RxFrm[485], SlotNum[19])-->PUSCHGrantNum[1]======
[08-26 12:19:21.350][INFO ]  NrOfSymbols[13]  ResourceAllocType[1]  NrOfRBGs[0]  RBStart[0]  RBSize[20]  RBGIndex(0-4)[0, 0, 0, 0, 0]
[08-26 12:19:21.350][INFO ]  nRNTI[17022]  nUEId[0]   BWPSize[273]  nBWPStart[0]  nSubcSpacing[1]  nCpType[0]  nULType[0]  nMcsTable[0]
[08-26 12:19:21.350][INFO ]  TBSize0[357] TBSize1[0] RBGSize[0]  RV0[0] RV1[0] HARQID[0]  NDI0[0] NDI1[0] MappingType[0]
[08-26 12:19:21.350][INFO ]  MCS[8]   TransPrecode[0]  TransmissionScheme[0]  NrOfLayers[1]  PortIndex(0-3)[0, 0, 1, 1]
[08-26 12:19:21.350][INFO ]  DMRSConfigType[0]  NrOfCDMs[2]  NrOfDMRSSymbols[1]  DMRSAddPos[2]  PTRSPresent[0]  NrOfPTRSPorts[0]  PTRSTimeDensity[0]
[08-26 12:19:21.350][INFO ]  nPTRSPortIndex0[0]  nPTRSPortIndex1[0]  nNrOfDMRSAssPTRS[0], nNrOfDMRSAssPTRS[0]  nPTRSFreqDensity[0]  nPTRSReOffset[0]
[08-26 12:19:21.350][INFO ]  nNid[41]  nSCID[0]  nNIDnSCID[41]  NrOfAntennaPorts[1]  VRBtoPRB[0]  RBBundleSize[0]  PMI[0]  StartSymbolIndex[0]
[08-26 12:19:21.350][INFO ]  nCodebookType[0]  nEpreRatioOfPDSCHToPTRS[0]  nEpreRatioOfDmrsToSSB[0]
[08-26 12:19:21.350][INFO ]==========================================================================
[08-26 12:19:21.350][INFO ]  NrOfSymbols[12]  ResourceAllocType[1]  NrOfRBGs[0]  RBStart[18]  RBSize[4]  RBGIndex(0-4)[0, 0, 0, 0, 0]
[08-26 12:19:21.350][INFO ]  TBSize[63]  RBGSize[0]  RV[0]  HARQID[0]  NDI[1]  MappingType[0]
[08-26 12:19:21.350][INFO ]FH_PUSCH_RX, CellIdx[0] FPGAslot[485,9,0] slotIdx[9718] gPkt[11960]
[08-26 12:19:21.350][INFO ]  DMRSConfigType[0]  NrOfCDMs[2]  NrOfDMRSSymbols[1]  DMRSAddPos[2]  PTRSPresent[0]  NrOfPTRSPorts[0]  PTRSTimeDensity[0]
[08-26 12:19:21.350][INFO ]  nPTRSPortIndex0[0]  nPTRSPortIndex1[0]  nPTRSFreqDensity[0]  nPTRSReOffset[0] nTpPi2BPSK[0]  nTPPuschID[0]
[08-26 12:19:21.350][INFO ]  AlphaScaling[0] BetaOffsetACKIndex[0] nAck[0]
[08-26 12:19:21.350][INFO ]==========================================================================
[08-26 12:19:21.350][INFO ]ul_config_req, RBSize[4] Layer[1] ULSymb[12] TotalDMRSSym[3] McsTable[0] tbsize[63], ModeOrder[2]
[08-26 12:19:21.350][INFO ]ZQ_PDCCH_DCI1_1 phy_dl_pdcch_dldci_task, nCellIdx[0] nCtxNum[1] nSlotAdvIdx[9721] nSlotInFrame[1] nPDCCHnumDLDCI[1] nPHYCellID[41]
[08-26 12:19:21.350][INFO ]ZQ_PDCCH_DCI1_1 : E[432] K[63] N[512]

[08-26 12:19:21.355][INFO ][TTI_START]: SlotIdx[9730] CellTiming[0]
[08-26 12:19:21.355][INFO ]ZQ_PDCCH_DCI1_1 phy_dl_pdcch_dldci_task, nCellIdx[0] nCtxNum[0] nSlotAdvIdx[9732] nSlotInFrame[12] nPDCCHnumDLDCI[0] nPHYCellID[41]
[08-26 12:19:21.355][INFO ]FH_PUSCH_RX, CellIdx[0] FPGAslot[486,4,1] slotIdx[9729] gPkt[11971]
[08-26 12:19:21.355][INFO ]Rx_F0_funcl, CRNTI[17021] slot[9] StartSym[12] Nsym[2] m0[0] PayloadLen[1] sr_check[0] pucch_sc[192] PRBIdx(0,1)[0,272] bDtx[0] SrPrsnt[0] Payload[128]
[08-26 12:19:21.355][INFO ]PUCCH_Format0-RNTI[17021](486, 9)  Dtx[0] UciBits[0] 128, PayloadLen[1], SRPresent[0]
[08-26 12:19:21.355][INFO ]eBBUPOOL_UL_POST, CellIdx[0] slot[9729] SlotAdvIdx[9729] iCtx[1]
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历史记录

#1 - 2025-09-02 18:14 - 雪峰 赖

MSG4的PDSCH 对应的PUCCH 的Harq ACK的K1 配置为4，目前PHY无法支持，只能支持大于5的场景

#2 - 2025-09-02 18:28 - 雪峰 赖

- 状态 从 新建 变更为 进行中

文件

img_v3_02ph_292fa9ad-15b7-4f82-a8b6-023d4880f7fg.jpg	631 KB	2025-08-26	赵 强