

测试环境 :
[gNB]192.168.2.106
该问题在定位ecpri射频环回，上行接收无数据导致挂死问题时出现

PHY&Testmac版本：/home/wangyongwei/dev2_all_0205/HT-5G NR-B02_1123/source_code/240/fr/pack/
FPGA版本：-
DRV版本：-

“ =====PDSCH FEC ENCODE TX HEADER===[sfn=21 subfn=6 slotNum=1]===== ”
无任何相关的上下文，仅有一条编码头的打印，初步怀疑是zlog打印缓存问题，待后续观察

```
[DEBUG]Func:phy_bbupool_update_multi_cell_status,  nSfIdx[1116]

[INFO ]nr5g_gnb_phy2mac_api_proc_send_api_list:  phyInstance: 0,  msgType: 16,  frameNumber: 55,  slotNumber: 17,  status: 0,
isRealTime: 1
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbupool_task_dl_config]  CellId[0]  Slot[1116]  SlotAdvIdx[1118]  Ctx[2]
[DEBUG]phy_fpga_dl_set_remap_buffer,  nSlotIdx[1116],  nSlotAdvIdx[1118],  bufIdx[6],  oneSymDataSize[13104],  nPktLen[26240]
!!!!!!!!!!!!!!!![DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=21  subfn=6  slotNum=1]=====
===!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
[DEBUG]phy_ul_pusch_decode_task_func,  slotIdx[1114],  cbNum[12],  nCbAddrSpaceLen[64],  qm[2],  nDecodeOutLen[12072],pduSize[
72888]
[DEBUG]---3.1--sTimeRec.drvLoopCnt=73183363
[DEBUG]---3.2--sTimeRec.drvLoopCnt=73183363
[DEBUG]pusch_decode_task_func[slotIdx(1114),CWNum[1], 1st half deal time[39.008000], 2nd half deal time[0.468000], saturate
ShiftTime[31.481000]

[INFO ]phy_dl_pdsch_rs_task,  nCellIdx[0],  nSlotAdvIdx[1118],  nCtxNum[2],  nGroup[1],  nSlotInFrame[0]
```

跳变前后的DL CONFIG中slot号是正常的

```
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbpool_task_dl_config] CellId[0] Slot[1109] SlotAdvIdx[1111] Ctx[3]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=55 subfn=5 slotNum=1]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbpool_task_dl_config] CellId[0] Slot[1110] SlotAdvIdx[1112] Ctx[0]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=55 subfn=6 slotNum=0]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbpool_task_dl_config] CellId[0] Slot[1111] SlotAdvIdx[1113] Ctx[1]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=55 subfn=6 slotNum=1]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbpool_task_dl_config] CellId[0] Slot[1112] SlotAdvIdx[1114] Ctx[2]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=55 subfn=7 slotNum=0]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbpool_task_dl_config] CellId[0] Slot[1113] SlotAdvIdx[1115] Ctx[3]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=55 subfn=7 slotNum=1]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbpool_task_dl_config] CellId[0] Slot[1114] SlotAdvIdx[1116] Ctx[0]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=55 subfn=8 slotNum=0]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbpool_task_dl_config] CellId[0] Slot[1115] SlotAdvIdx[1117] Ctx[1]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=55 subfn=8 slotNum=1]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbpool_task_dl_config] CellId[0] Slot[1116] SlotAdvIdx[1118] Ctx[2]
```

[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=21 subfn=6 slotNum=1]=====

[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=55 subfn=9 slotNum=0]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbupool_task_dl_config] CellId[0] Slot[1117] SlotAdvIdx[1119] Ctx[3]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=55 subfn=9 slotNum=1]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbupool_task_dl_config] CellId[0] Slot[1118] SlotAdvIdx[1120] Ctx[0]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=56 subfn=0 slotNum=0]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbupool_task_dl_config] CellId[0] Slot[1119] SlotAdvIdx[1121] Ctx[1]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=56 subfn=0 slotNum=1]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbupool_task_dl_config] CellId[0] Slot[1120] SlotAdvIdx[1122] Ctx[2]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=56 subfn=1 slotNum=0]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbupool_task_dl_config] CellId[0] Slot[1121] SlotAdvIdx[1123] Ctx[3]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=56 subfn=1 slotNum=1]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbupool_task_dl_config] CellId[0] Slot[1122] SlotAdvIdx[1124] Ctx[0]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=56 subfn=2 slotNum=0]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbupool_task_dl_config] CellId[0] Slot[1123] SlotAdvIdx[1125] Ctx[1]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=56 subfn=2 slotNum=1]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbupool_task_dl_config] CellId[0] Slot[1124] SlotAdvIdx[1126] Ctx[2]
[DEBUG]=====PDSCH FEC ENCODE TX HEADER===[sfn=56 subfn=3 slotNum=0]=====
[DEBUG]---- 0_DL_L1_CONFIG [phy_gnb_bbupool_task_dl_config] CellId[0] Slot[1125] SlotAdvIdx[1127] Ctx[3]

历史记录

#1 - 2021-02-07 16:53 - guo hanlin

- 状态从新建变更为进行中

#2 - 2021-02-18 09:40 - guo hanlin

- 状态从进行中变更为挂起