

3.0基站产品测试 - 错误 #4597

ICIC特性，高干扰+边缘ue上行调度起始RB有问题，从0起始，到30，期望结果是从213起始，到243

2025-12-12 10:02 - 王 旭初

状态:	新建	开始日期:	2025-12-12
优先级:	一般	计划完成日期:	
指派给:	李 宇哲	% 完成:	0%
类别:		预期时间:	0.00 小时
目标版本:		耗时:	0.00 小时
问题归属:	DU	目标解决问题版本:	Rel_3.1.4
发现问题版本:	Rel_3.1.3		
<div>描述</div> <div><pre>--11-25T08:01:32.962][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.963][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.963][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.965][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.966][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.967][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.968][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.970][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.971][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.972][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.973][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.973][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.975][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.976][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.977][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.978][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.978][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.980][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.981][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.982][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3] --11-25T08:01:32.983][YS_DL][t:541386840944][rg_sch_pusch_mgr.c:843][DBG][CORE-4]rgSCHCmnUlRbAllocForUe:Allocctr response for CellId[1] UE[17017] startRB[0] numRB[30] raType[1] icicEnable[2] icicState[3]</pre></div>			

历史记录

#1 - 2025-12-12 10:32 - 李 宇哲

- 文件 屏幕截图 2025-12-12 103155.png 已添加

之前组内走查代码修改部分逻辑未验证过，导致调度rb时，起始rb获取到的固定为0已完善

<pre>if (tmpStartIdx != 0xFFFF && tmpMaxNum != 0) { bwpRangeInfo.bwpLoc = tmpStartIdx; bwpRangeInfo.bwpStartRB = tmpStartIdx; bwpRangeInfo.bwpEndRB = bwpRangeInfo.bwpStartRB + tmpMaxNum - 1; bwpRangeInfo.bwpLoc = RGSCH_MAX(bwpRangeInfo.bwpLoc, D1SchStartPrb) bwpRangeInfo.bwpStartRB = RGSCH_MAX(bwpRangeInfo.bwpStartRB, D1SchStar bwpRangeInfo.bwpEndRB = RGSCH_MIN(bwpRangeInfo.bwpEndRB, (D1SchStar</pre>	<pre>1583 1584 1585 1586+ 1587 1588 1589 1590 1591 1592 1593</pre>	<pre>if (tmpStartIdx != 0xFFFF && tmpMaxNum != 0) { //bwpRangeInfo.bwpLoc = tmpStartIdx; bwpRangeInfo.bwpStartRB = tmpStartIdx; bwpRangeInfo.bwpEndRB = bwpRangeInfo.bwpStartRB + tmpMaxNum - 1; bwpRangeInfo.bwpLoc = RGSCH_MAX(bwpRangeInfo.bwpLoc, D1SchStartPrb) bwpRangeInfo.bwpStartRB = RGSCH_MAX(bwpRangeInfo.bwpStartRB, D1SchS bwpRangeInfo.bwpEndRB = RGSCH_MIN(bwpRangeInfo.bwpEndRB, (D1SchStar</pre>	<pre>1583 1584 1585 1586+ 1587 1588 1589 1590 1591 1592 1593</pre>
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文件

其实rb.jpg	835 KB	2025-12-12	王 旭初
屏幕截图 2025-12-12 103155.png	35.4 KB	2025-12-12	李 宇哲